REMARKS

Claims 1-65 are pending in the present application.

In the office action mailed November 9, 2005 (the "Office Action"), the Examiner objected to claims 41 and 63-65 based on informalities. The Examiner also rejected claims 1, 4, 20, 21, 24, 25, 44, 45, 48, 51, 57, and 58 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,484,268 to Tamura *et al.* (the "Tamura patent"). Claim 26 was rejected under 35 U.S.C. 103(a) as being unpatentable over the Tamura patent in view of U.S. Patent No. 4,019,153 to Cox, Jr. *et al.* (the Cox patent") and claim 40 was rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,173,432 to Harrison (the "Harrison patent") in view of the Tamura patent. Claim 41 was rejected under 35 U.S.C. 103(a) as being unpatentable over the Harrison patent in view of the Tamura patent, and further in view of U.S. Patent Application Publication No. 20020078294 to Tsuchida *et al.* (the "Tsuchida application"). Finally, claims 42 and 43 were rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,792,516 to Mastornarde *et al.* (the "Mastornarde patent") in view of the Harrison patent, and in further view of the Tamura patent. Claims 63-65 were allowed by the Examiner, and claims 2, 3, 5-11, 22, 23, 27-31, 46, 47, 49, 50, 52-56, and 59-62 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form.

With respect to the Examiner's objection to claim 41, claim 41 has been amended to recite "double data rate synchronous dynamic random access memory" instead of "DDR SDRAM." A description of a double data rate synchronous dynamic random access memory is provided in the present specification at page 20-page 24-line 28, and is described with reference to Figure 9. Claim 43 has been similarly amended. The Examiner's objection to claim 41 should now be withdrawn.

With respect to the Examiner's objection to claims 63-65, claim 63 has been amended as suggested by the Examiner. The objection to claims 63-65 should now be withdrawn.

As previously mentioned, claims 1, 4, 20, 21, 24, 25, 44, 45, 48, 51, 57, and 58 under 35 U.S.C. 103(a) as being unpatentable over the Tamura patent.

Claims 1, 4, 20, 21, 24, 25, 44, 45, 48, 51, 57, and 58 are patentable over the Tamura patent because the Examiner failed to establish a *prima facie* case of obviousness.

With respect to claim 1, the Examiner argues that, "although Tamura does not explicitly disclose the comparison of the current and future data signals directly, as broadly as claimed, it is inherent, implied, or at least obvious that the phase shifted clock signal has a phase shift which is a *function* of the current and future data signals." (Emphasis in original). *See* the Office Action at page 4. The argument set forth by the Examiner, however, does not satisfy the elements for establishing a *prima facie* case of obviousness. As set forth in the MPEP section 2143, a *prima facie* case of obviousness requires that (1) there is some suggestion or motivation to modify the reference or to combine teachings; (2) there must be a reasonable expectation of success; and (3) the prior art reference must teach or suggest all the claim limitations. The Examiner's argument fails to set forth at least the first and third elements. That is, the Examiner has failed to provide any motivation to modify the teachings of the Tamura patent, and has further failed to identify the teaching or suggestion for all of the claim limitations. The Examiner relies on the same reasoning in rejecting claims 40, 42, 48, 51, and 63, and the following remarks apply to those claims as well.

The Examiner's position, which was previously presented, is that because of the breadth of the claim, it would have been obvious based on the explicit teachings of the Tamura patent to generate a phase shifted clock signal relative to the input clock signal that is a function of the current and respective future data signals, as recited in claim 1. The Examiner does not rely on any additional reference to teach elements not explicitly disclosed in the Tamura patent nor does the Examiner provide any motivation or cite any knowledge generally available in the art for modifying the Tamura patent. The Examiner's argument for rejecting the claims is simply that the claims are obvious because it would have been obvious. This argument, however, does not meet the requirements for a *prima facie* case of obviousness.

Additionally, even if it is assumed that the teachings of the Tamura patent could be modified as suggested by the Examiner, it would render the signal transmission system described in the Tamura patent unfit for its intended use.

The Tamura patent teaches adjusting the timing (i.e., phase) of clock signals for input latches or output latches so that, in the case of input latches, data that arrives at different times are latched by a respective clock signal tailored to the timing skew of the particular data so that the data can be latched at the correct time. In determining the amount of timing adjustment

for each clock signal clocking a respective input latch, a phase comparison is made between the incoming data and a delayed version of a complementary clock signal of a master clock signal. A first adjustable delay is used to provide the delayed complementary clock signal to the phase and is adjusted so that delayed complementary clock signal is in phase with the incoming data signal. A second adjustable delay providing a delayed true clock signal based on the master clock signal is adjusted to provide the same delay as the first adjustable delay. Under this condition, the delayed true clock signal corresponds to an ideal clock signal for clocking the particular input latch.

The determination of the amount of delay used for providing a delayed true clock signal for clocking a respective input latch is based on comparing a *current* data signal with a clock signal 180 degrees out of phase from the true clock signal used to clock the input latch. Modifying the system to compare the phase of a current data signal with the phase of a future data signal, as suggested by the Examiner, and adjusting an adjustable delay so that the current data signal and the future data signal are in phase only results in delaying the current data to be provided at the same time as the future data. This does not address the problems discussed in the Tamura patent of using one clock signal to clock input latches for all of the data lines, that is, the delays (skew) of respective data signal lines are different enough that not all of the data will be latched properly by one clock signal. The solution presented in the Tamura patent is to tailor the clock signal clocking a respective input latch to the delay of the particular signal line so that the data is latched at the correct time. The problem and solution presented are discussed with respect to Figures 10-19, and described at col. 17, line 21-col. 21, line 39. Modifying the system described in the Tamura patent as set forth in the Examiner's argument would not solve the problem the system was intended to solve.

The problems addressed by embodiments of the present invention are different than those resolved by the system of the Tamura patent. In particular, loading of the power supply may cause variations in delay for driving output data signals. For example, where only one or two data signals have logic transitions from current data to future data, the power supply will likely have sufficient margin to drive all of the output signals to meet device performance specifications. However, where several of the data signals have logic transitions, the power supply will be significantly loaded, and a much longer delay in driving the respective output

signals may result. To address this problem, the clock signals clocking the output drivers are adjusted according to the anticipated loading of the power supply as determined from current and future data or read and corresponding output data signals. For example, in the case where loading is not an issue, a normal delay is added to the clock signal clocking the output drivers. However, where loading is an issue, such as when several of the data signals will be transitioning, less delay is added to the clock signal so that the output driver can be clocked earlier to accommodate the additional delay due to power supply loading.

The different problems addressed by the Tamura patent and embodiments of the present invention reflect part of the reason why modifying the system of the Tamura patent would not be desirable, and in fact, if modified as suggested by the Examiner, would render the system unfit for its intended purpose.

With respect to claims 21, 44, and 57, the Examiner argues that the system described in the Tamura patent receives respective read and corresponding output data signals as shown by receiving a read data signal at time t0 and subsequently a corresponding output data signal at t0-1. However, the data signals received at times t0 and t0-1 are not analogous to respective read and corresponding output data signals because the Tamura patent describes a system that provides a delay based on only a current data signal and a clock signal. As recited in claim 21, the phase shifted clock signal having a phase shift relative to the input clock signal that is a function of the respective read data *and* corresponding output data signals. In the Tamura patent, the system does not evaluate any data provided to the drive circuits 511-51n, but only evaluates the DD1-DDn signal already output by the respective drive circuit 511-51n. With respect to claims 44 and 57, the output delay is determined from the detected respective first *and* second logic states of each data signal, which is unlike the system in the Tamura patent which determines a respective clock delay based on only the received data signal.

For the foregoing reasons, claims 1, 21, 25, 44, 48, 51, and 57 are patentable over the Tamura patent, and consequently, the rejection of these claims under 35 U.S.C. 103(a) should be withdrawn. Claims 4 and 20, which depend from claim 1, claim 24, which depends from claim 21, claim 45, which depends on claim 44, and claim 58, which depends from claim 57 are similarly patentable because of their dependency from a respective allowable base claim.

Therefore, the rejection of claims 1, 4, 20, 21, 24, 25, 44, 45, 48, 51, 57, and 58 under 35 U.S.C. 103(a) should be withdrawn.

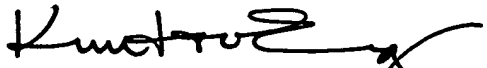
As previously mentioned, claims 26 and 40-43 were rejected under various combinations of the Tamura patent in view of the Harrison patent, the Mastornarde patent, and the Tsuchida application. None of these references make up for the deficiencies of the Tamura patent previously discussed. Therefore, claims 26 and 40-43 are patentable because the combined teachings of the cited references do not teach or suggest the combination of limitations recited by the respective claims. Therefore, the rejection of claims 26 and 40-43 under 35 U.S.C. 103(a) should be withdrawn.

With reference to withdrawn claims 12-19 and 32-39, consideration of these claims is requested in response to the allowance of generic claims 1-5, 25, and 26.

All of the claims pending in the present application are in condition for allowance. Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,

DORSEY & WHITNEY LLP



Kimton N. Eng
Registration No. 43,605
Telephone No. (206) 903-8718

KNE:ajs

Enclosures:
Postcard
Fee Transmittal Sheet (+ copy)

DORSEY & WHITNEY LLP
1420 Fifth Avenue, Suite 3400
Seattle, WA 98101-4010
(206) 903-8800 (telephone)
(206) 903-8820 (fax)

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